Board Level Application Notes for DFN and QFN Packages

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APPLICATION NOTE

INTRODUCTION

Various ON Semiconductor components are packaged in an advanced Dual or Quad Flat−Pack No−Lead package (DFN/QFN). The DFN/QFN platform represents the latest in surface mount packaging technology, it is important that the design of the Mounting Pads of the Printed Circuit Board (PCB), Soldermask and Stencil pattern, along with the assembly process, all follow the suggested guidelines outlined in this document.

DFN/QFN Package Overview

The DFN/QFN platform offers a versatility which allows either a single or multiple semiconductor devices to be connected together within a leadless package. This packaging flexibility is illustrated in Figure 1 where four devices are packaged together with a custom pad configuration.

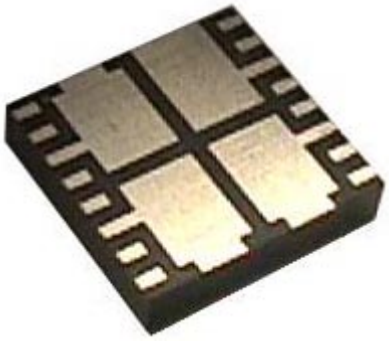

Figure 1. The Underside of a 4−Chip 16 Pin DFN Package

Figure 2 illustrates a single site DFN semiconductor device package which allows for a large device.

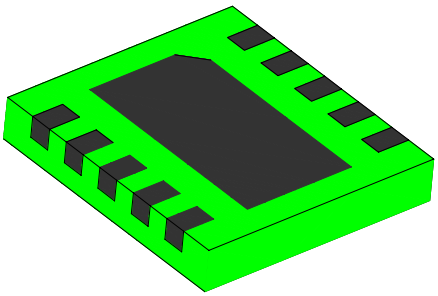

Figure 2. The Underside of a Single−Chip 10 Pin DFN Package

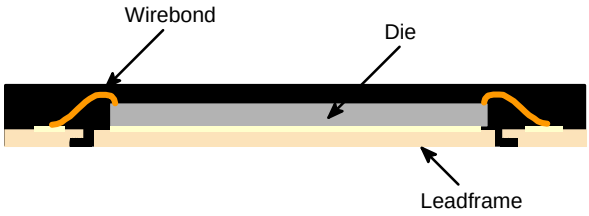

Figure 3. Cross−Section of a Single−Chip DFN Package

Figure 3 illustrates how the package height is reduced to a minimum by having both the die and wirebond pads on the same plane. When mounted, the leads are directly attached to the board without a space−consuming standoff, which is inherent in a leaded package.

Figure 3 also illustrates how the ends of the leads are flush with the edge of the package. This configuration allows for the maximum die size within a given footprint, while maximizing the board space efficiency.

In addition to these features, the DFN/QFN package has excellent thermal dissipation and reduced electrical parasitics due to its efficient and compact design.

Printed Circuit Board Solder Pad Design Guidelines

Refer to the case outline (specification sheet) drawing for the specific DFN/QFN package to be mounted. Based on the nominal package footprint dimensions from the case drawing. The PCB mounting pads need to be larger than the nominal package footprint (see Figure 4).

Note: On the occasion that there is not enough room to grow the PCB mounting pads per these guidelines, the recommendation would be to come as close to these guidelines as possible.

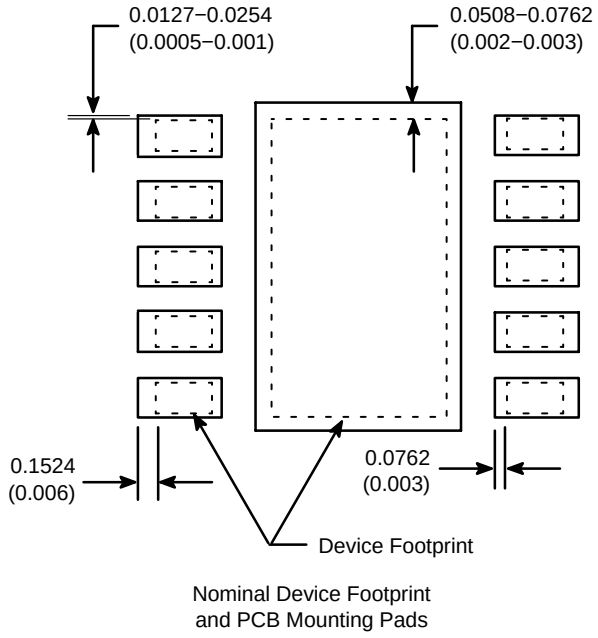

Figure 4. 10 Pin DFN Package Footprint Shown with PCB Mounting Pads

Printed Circuit Board Solder Mask Design Guidelines

SMD and NSMD Pad Configurations

There are two different types of PCB pad configurations commonly used for surface mount leadless DFN/QFN style packages. The different configurations are:

1. Non Solder Masked Defined (NSMD)
2. Solder Masked Defined (SMD)

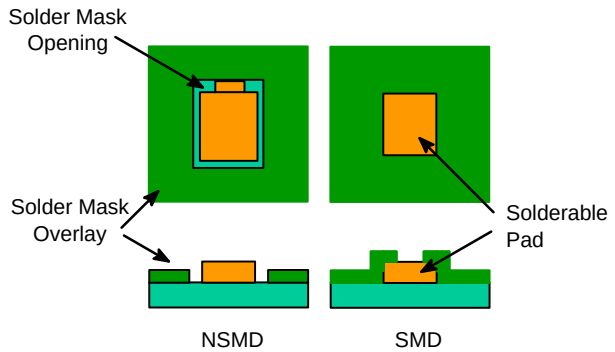

Figure 5. Comparison of NSMD vs. SMD Pads

As their titles describe, the NSMD contact pads have the solder mask pulled away from the solderable metallization, while the SMD pads have the solder mask over the edge of the metallization, as shown in Figure 5. With the SMD Pads, the solder mask restricts the flow of solder paste on the top of the metallization which prevents the solder from flowing along the side of the metal pad. This is different from the NSMD configuration where the solder will flow around both the top and the sides of the metallization.

Typically, the NSMD pads are preferred over the SMD configuration since defining the location and size of the copper pad is easier to control than the solder mask. This is based on the fact that the copper etching process is capable of a tighter tolerance than the solder masking process. This also allows for visual inspection of solder fillet.

In addition, the SMD pads will inherently create a stress concentration point where the solder wets to the pad on top of the lead. This stress concentration point is reduced when the solder is allowed to flow down the sides of the leads in the NSMD configuration.

Printed Circuit Board Solder Mask Design Guidelines

When dimensionally possible, the solder mask should be located within a range of 0.0762–0.1270 mm (0.003–0.005 in) away from the edge of the PCB mounting pad (see Figure 6). This spacing is used to compensate for the registration tolerances of the solder mask, as well as to insure that the solder is not inhibited by the mask as it reflows along the sides of the metal pad.

The solder mask web (between openings) is the controlling factor in the pattern, and needs to be held to a minimum of 0.1016 mm (0.004 in). This minimum is the current PCB suppliers standard minimum web for manufacturability. Because of this web restriction, solder mask openings around PCB pads may need to be less than the recommended shown. Whenever possible, keeping to the range given will provide for the best results.

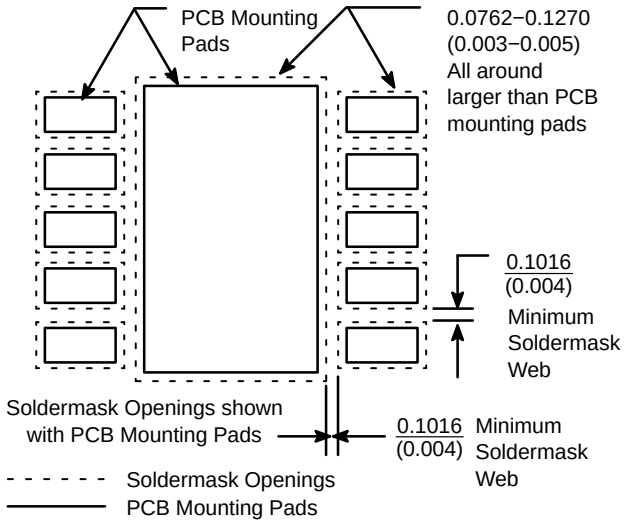

Figure 6. Typical DFN Package − PCB Mounting Pads Shown with Soldermask Openings

DFN/QFN Board Mounting Process

The DFN/QFN board mounting process is optimized by first defining and controlling the following.

1. Solderable metallization on the PCB contacts.
2. Choice of proper solder paste.
3. Solder paste on the PCB.
4. Package placement.
5. Reflow of the solder paste.
6. Final solder joint inspection.

Recommendations for each of these processes are located below.

PCB Solderable Metallization

There are currently three common solderable coatings which are used for PCB surface mount devices. In any case, it is imperative that the coating is uniform, conforming, and free of impurities to insure a consistant solderable system.

The first coating consists of an Organic Solderability Protectant (OSP) applied over the bare copper feature. OSP coating assists in reducing oxidation in order to preserve the copper metallization for soldering. It allows for multiple passes through reflow ovens without degradation of the solderability. The OSP coating is dissolved by the flux when the solder paste is applied to the metal features. Coating thickness recommended by OSP manufacturers is between 0.25 and 0.35 microns.

The second coating is a metalized coating which consists of plated electroless nickel over the copper pad, followed by a coat of immersion gold. The thickness of the electroless nickel layer is determined by the allowable internal material stresses and the temperature excursions the board will be subjected to throughout its lifetime. Even though the gold metallization is typically a self−limiting process, the thickness should be at least 0.05 μm thick, and not consist of more than 5% of the overall solder volume. Having excessive gold in the solder joint can create gold embitterment which may affect the reliability of the joint.

The third is a tin−lead coating, commonly called Hot Air Solder Level (HASL).This type of PCB pad finish is not recommended for DFN/QFN type packages. The major issue is the inability to consistently control the amount of solder coating applied to each pad. This results in dome−shaped pads of various heights. As the industry drives for finer and finer pitch, solder bridging becomes a common problem between mounting pads.

Solder Type

Solder paste such as Cookson Electronics' WS3060 with a Type 3 or smaller sphere size is recommended. The WS3060 has a water−soluble flux for cleaning. Cookson Electronics' PNC0106A can be used if a no−clean flux is preferred.

Solder Screening onto the PCB

Stencil screening the solder paste onto the PCB is commonly used in the industry. The recommended stencil thickness used is 0.075 mm to 0.127 mm (0.003 in to 0.005 in). The sidewalls of the stencil openings should be tapered approximately 5° to facilitate the release of the paste when the stencil is removed from the PCB.

The stencil opening should be the same size as the PCB mounting pad. The exception is when there is a large center flag on the device. Then the stencil opening should allow for 70−80% coverage of the PCB mounting pad. This opening should also be divided into smaller cavities to aid in the flow of solder during the reflow process (see Figure 7). Dividing the larger die pads into smaller screen openings reduces the risk of solder voiding and allows the solder joints for the smaller terminal pads to be at the same height as the larger ones.

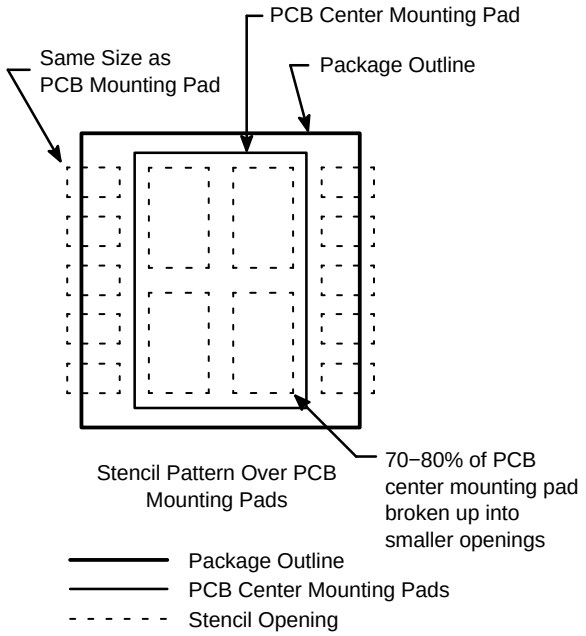

Figure 7. Typical DFN Package with Stencil Openings Shown Over PCB Mounting Pads

Package Placement onto the PCB

Pick and place equipment with the standard tolerance of ±0.05 mm (0.002 in) or better is recommended. The package will tend to center itself and correct for slight placement errors during the reflow process due to the surface tension of the solder.

Solder Reflow

Once the package is placed on the PC board along with the solder paste, a standard surface mount reflow process can be used to mount the part. Figures 8 and 9 are examples of standard reflow profiles for standard eutectic and lead free solder alloys.

The exact profile will be determined, and is available, by the manufacture of the paste since the chemistry and viscosity of the flux matrix will vary. These variations will require small changes in the profile in order to achieve an optimized process.

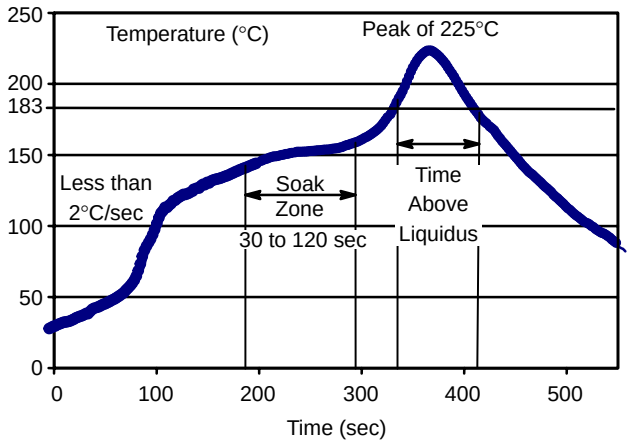

Figure 8. Typical Reflow Profile for Eutectic Tin/Lead Solder

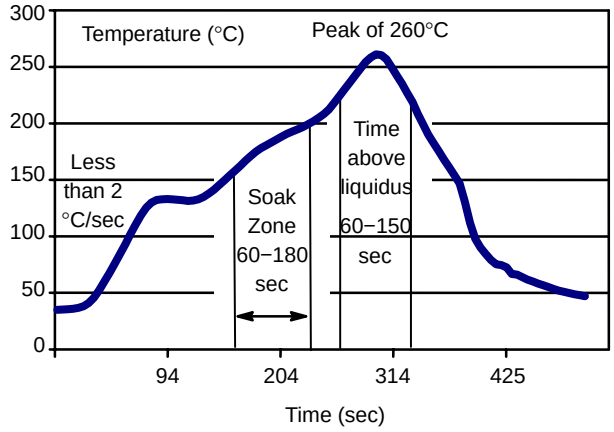

Figure 9. Typical Reflow Profile for Pb−Free Solder

In general, the temperature of the part should be raised not more than 2°C/sec during the initial stages of the reflow profile. The soak zone then occurs when the part is approximately 150°C and should last for 60 to 180 seconds for Pb−free profiles (30−120 sec for Eutectic profiles). Typically, extending the time in the soak zone will reduce the risk of voiding within the solder. The temperature is then raised and will be above the liquidus of the solder for 60 to 150 seconds for Pb−free profiles (30−100 sec for Eutectic profiles) depending on the mass of the board. The peak temperature of the profile should be between 245 and 260°C for Pb−free solder alloys (205−225°C) for eutectic solders.

If required, removal of the residual solder flux can be completed by using the recommended procedures set forth by the flux manufacturer.

Final Solder Inspection

The inspection of the solder joints is commonly performed with the use of an X−ray inspection system. With this tool, one can locate defects such as shorts between pads, open contacts, voids within the solder as well as any extraneous solder.

In addition to searching for defects, the mounted device should be rotated on its side to inspect the sides of the solder joints with an X−ray inspection system. The solder joints should have enough solder volume with the proper stand−off height so that an “Hour Glass” shaped connection is not formed as shown below in Figure 10. “Hour Glass” solder joints are a reliability concern and must be avoided.

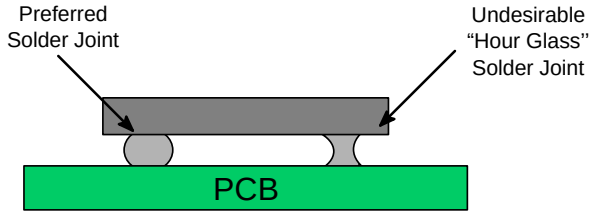

Figure 10. Side View of DFN Illustrating Preferred and Undesirable Solder Joints

Rework Procedure

Due to the fact that the DFN/QFN’s are leadless devices, the entire package must be removed from the PC board if there is an issue with the solder joints. It is important to minimize the chance of overheating neighboring devices during the removal of the package since the devices are typically in close proximity with each other.

Standard SMT rework systems are recommended for this procedure since the airflow and temperature gradients can be carefully controlled. It is also recommend that the PC board be placed in an oven at 125°C for four to eight hours prior to heating the parts to remove excess moisture from the packages. In order to control the region which will be exposed to reflow temperatures, the board should be heated to a 100°C by conduction through the backside of the board in the location of the device. Typically, heating nozzles are then used to increase the temperature locally.

Once the device’s solder joints are heated above their liquidus temperature, the package is quickly removed and the pads on the PC board are cleaned. The cleaning of the pads is typically performed with a blade−style conductive tool with a desoldering braid. A no clean flux is used during this process in order to simplify the procedure.

Solder paste is then deposited or screened onto the site in preparation of mounting a new device. Due to the close proximity of the neighboring packages in most PC board configurations, a miniature stencil for the individual component is typically required. The same stencil design that was originally used to mount the package can be applied to the mini−stencil for redressing the pads.

Due to the small pad configurations of the DFN/QFN, and since the pads are on the underside of the package, a manual pick and place procedure without the aid of magnification is not recommended. A dual image optical system where the underside of the package can be aligned to the PC board should be used instead.

Reflowing the component onto the board can be accomplished by either passing the board through the original reflow profile, or by selectively heating the package with the same process that was used to remove it. The benefit with subjecting the entire board to a second reflow is that the new part will be mounted consistently and by a profile that is already defined. The disadvantage is that all of the other devices mounted with the same solder type will be reflowed for a second time. If subjecting all of the parts to a second reflow is either a concern or unacceptable for a specific application, than the localized reflow option would be the recommended procedure.

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